FPGA Implementation of MIMO Module

1. INTRODUCTION

Radio transmissions traditionally use one antenna at the transmitter and one antenna at the receiver. This system is termed **Single Input Single Output (SISO).** Both the transmitter and the receiver have one RF chain (that's coder and modulator). SISO is relatively simple and cheap to implement and it has been used age long since the birth of radio technology. It is used in radio and TV broadcast and our personal wireless technologies (e.g. Wi-Fi and Bluetooth). Figure 1.1 shows SISO Model. One antenna at both the transmitter and the receiver. employs no diversity technique.

Figure 1.1 Single Input Single Output (SISO)

To improve performance, a multiple antenna technique has been developed. A system which uses a single antenna at the transmitter and multiple antennas at the receiver are named **Single Input Multiple Output (SIMO).** The receiver can either choose the best antenna to receive a stronger signal or combine signals from all antennas in such a way that maximizes SNR (Signal to Noise Ratio). The first technique is known as switched diversity or selection diversity. The latter is known as maximal ratio combining (MRC).Figure 1.2 shows the SIMO Model, One antenna at the transmitter, two antennas the receiver. Employs a receive diversity technique
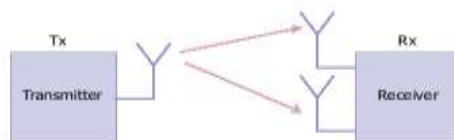

Figure 1.2 Single Input Multiple Output (SIMO)

A system which uses multiple antennas at the transmitter and a single antenna at the receiver is named as Multiple Input Single Output (MISO). A technique known as **Alamouti STC (Space Time Coding)** is employed at the transmitter with two antennas. STC allows the transmitter to transmit signals (information) both in time and space, meaning the information is transmitted by two antennas at two different times consecutively.

Multiple antennas (each with an RF chain) of either SIMO or MISO are usually placed at a base station (BS). This way, the cost of providing either a receive diversity (in SIMO) or transmit diversity (in MISO) can be shared by all subscriber stations (SSs) served by the BS. Two antennas at the transmitter, one antenna at the receiver, Employs a transmit diversity. Figure1.3 shows the MISO model.
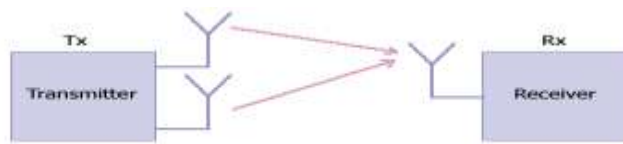

Figure1.3: Multiple Input Single Output (MISO)

To multiply throughput of a radio link, multiple antennas (and multiple RF chains accordingly) are put at both the transmitter and the receiver. This system is termed Multiple Input Multiple Output (MIMO). A MIMO system with similar count of antennas at both the transmitter and the receiver in a point-to-point (PTP) link is able to multiply the system throughput linearly with every additional antenna. For example, a 2x2 MIMO will double the throughput.
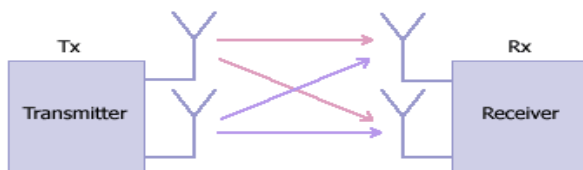

Figure: 1.4.Multiple Input Multiple Outputs (MIMO), 2x2

A MIMO system takes advantage of the spatial diversity that is obtained by spatially separated antennas in a dense multi path scattering environment. MIMO systems may be

implemented in a number of different ways to obtain either a diversity gain to combat signal fading, or to obtain a capacity gain.

Generally there are three categories of MIMO Techniques. The first aims to improve the power efficiency by maximizing spatial diversity. Such techniques include delay diversity, space-time block codes (STBC) [4], [5] and space-time trellis codes (STTC) [6]. The second class uses a layered approach to increase capacity. One popular example of such a system is V-BLAST suggested by Foschini *et al.* [7] where full spatial diversity is usually not achieved. Finally, the third type exploits the knowledge of channel at the transmitter. It decomposes the channel coefficient matrix using Singular Value Decomposition (SVD) and uses these decomposed unitary matrices as pre and post filters at the transmitter and the receiver to achieve near capacity [8].

In this paper, an efficient FPGA design of a (2x2) MIMO System (STBC) is presented. This paper is organized as follows. Section 2 presents about the number representation used in the design. Section 4 presents an overview of MIMO Systems. Section 3 described the design of MIMO .Section 5 discusses the results and we conclude in Section 6.

2.   Multiple Input Multiple Output

A third dimension, space, is introduced into the traditional frequency-time domain. The idea is to transmit multiple streams of data on multiple antennas at the same frequency, to increase throughput. Typically, multiple receiver antennas are used as well, since this configuration achieves high data rates, multiplied by the number of channels between either end. This principle is called Multiple Input Multiple Output (MIMO) [1]. There are two methods widely used for transmitting MIMO data. If the channel has a negligible error rate, we can send several data simultaneously over multiple antennas. This is known as spatial multiplexing, which utilizes the spectrum very efficiently. In contrast, if the environment has high error rate, we transmit the same data over multiple antennas. This is called as space-time coding. The purpose of this approach is to increase the diversity of MIMO to combat signal fading.

The essential purpose of a MIMO system is to determine which antenna is corresponding to which data on the receiver side. As shown in Figure 1, Rx1 receives data from all the transmitter antennas, Tx1, Tx2, and Tx3. Thus, we must have a special decoding algorithm to identify which antenna has transmitted which data to Rx1.[10]
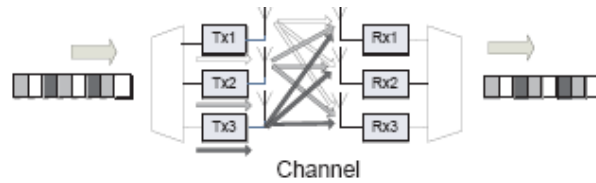
Channel

Figure 2.1: The MIMO Principle [1]

3. Number Representation

The number system being used in the project is floating point number representation, this is one of the important specification you should take care before starting the actually design. An 8 bit custom floating point format is used for representing the numbers.

Floating-point systems were developed to provide high resolution over a large dynamic range. Floating-point systems often can provide a solution when fixed-point systems, with their limited precision and dynamic range fail Floating-Point systems; however, bring a speed and complexity penalty. Most floating-point systems comply with the published single or double –precision IEEE floating –point standard A standard floating-point word consists of a sign-bit S, exponent e, and an unsigned (fractional) normalized mantissa m, arranged as follows: [3]

Sign Bit (S)	mantissa (m)	Exponent (e)
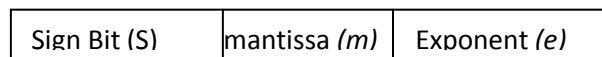
Algebraically, a floating-point word is represented by

$$X = - \quad \times \quad \times \qquad ..(2.1)$$

This is a signed magnitude format. The hidden one in the mantissa is not present in the binary coding of the floating point number. If the exponent is represented with E bits then the bias is selected to be

$$bias = \quad - \qquad ..(2.2$$

3.1 8 bit Custom floating point format

Custom floating point format is used, i.e. 3 bits are used for representing mantissa, 4 bits for exponent and the other is the sign bit. To illustrate, let us determine decimal equivalent of 3.75 in the 8 bit custom floating point format

Consider a floating point representation with sign bit, E=4 bit exponent width and M=3-bit for mantissa (not including the hidden one).Let us now determine the representation of 3.75_{10} in this (1, 4, 3) floating point format using (4. 13) the bias is

$$bias = \qquad -$$

$$bias = \quad - = \quad - =$$

and mantissa needs to be normalized according to 1.m format i.e

$$3.75_{10} = 11.11_2 = 1.\underline{111} \times 2^3$$
$$| $$
$$mantissa(m)$$

The biased exponent is therefore represented with

E= 1+ bias= 1+7 = 1000_2

Finally, we can represent

3.75_{10} In the (1, 4, 3) floating point format with

Sign Bit(S)	Exponent (e)	Unsigned mantissa (m)
0	1000	111

Hence 3.75 = 01000111 in floating point format

Due to the large gate count capacity of current FPGA's the design of floating point arithmetic has become a viable option. In addition, the introduction of the embedded 18 x 18 bit array multiplier Xilinx Virtex 2, Spartan 3 and Altera Stratix FPGA device families allows an efficient design of custom floating point arithmetic.[10]

Floating point Multiplier and adder were developed according to the standard IEEE floating point algorithms.

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4. MIMO Architecture Design

The Top block of the entire system is shown in figure 4.1; it consists of the following Components Input and Output Memory (for storing input and output bit stream) MIMO Encoder (Alamouti, Space time encoder) 16 QAM Modulator16 QAM Demodulator, MIMO Decoder (space time decoder) and Wireless channel model. In the following section the design of each module and its design is been discussed in detail.
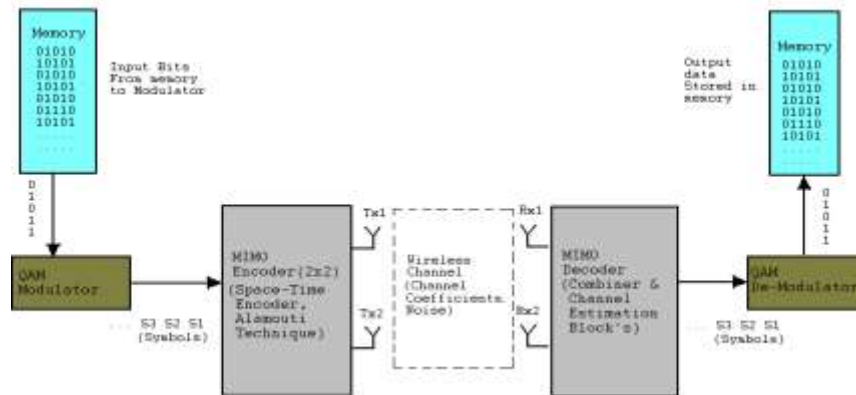

Figure 4.1: MIMO-Top Level Block Diagram

The input bit stream which is to be transmitted is stored in a text file, from where it is stored in a memory. And the output of the memory is the input of the modulator; similarly the output from demodulator is stored in the output memory.

The input Bits are stored in a memory, form where the bits are passed to the Modulator these bits acts as input to modulator. At every clock pulse bits stored in memory are passed through the modulator, which gives output symbols (i.e. real and imaginary values), in the same way at every trigger of clock the bits keep on passing from memory to modulator and the QAM demodulator, the output bits coming out of demodulator are stored in the output memory and a comparison is done between output and input memory to find bit error rate. The Modulation Scheme which is been employed is 16 QAM.

The MIMO Encoder Module is as shown in figure 4.2. The port connections are also shown in the figure below. Input to MIMO encoder comes from QAM modulator block.
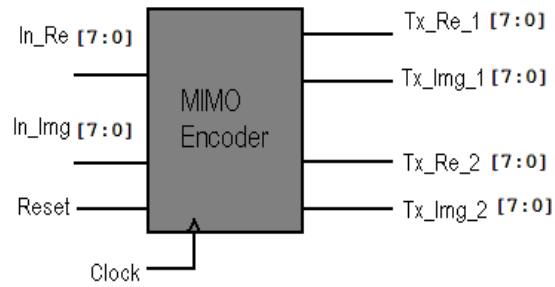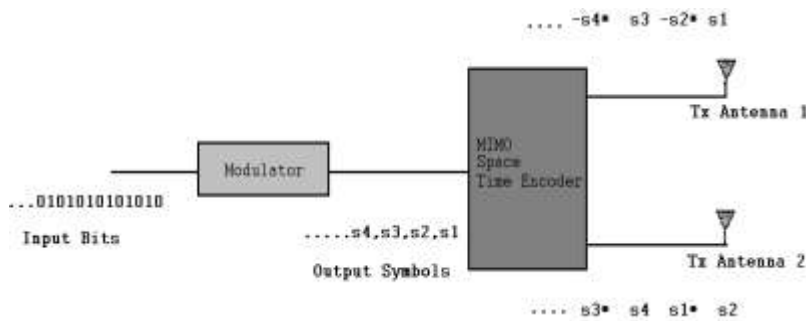
Figure 4.2: MIMO Encoder Module

Figure 4.3: MIMO Encoding and Transmitting scheme

The functionality of the encoder block is explained in the following steps,

- ➢ The output symbols coming from QAM modulator block, are the inputs to the MIMO encoder
- ➢ Symbols coming in the MIMO encoder are stored in a memory(buffer) , as it has to wait for a minimum of 2 symbols(i.e. S1, & S2) after that it encoder the symbols and transmits it, it can be seen in Figure 4.3
- ➢ symbols are encoded and then transmitted
- ➢ In a similar fashion all the symbols are transmitted.
- ➢ This achieves diversity gain
- ➢ Verilog HDL code i.e. been developed for the module , the results have been discussed in detail in next section
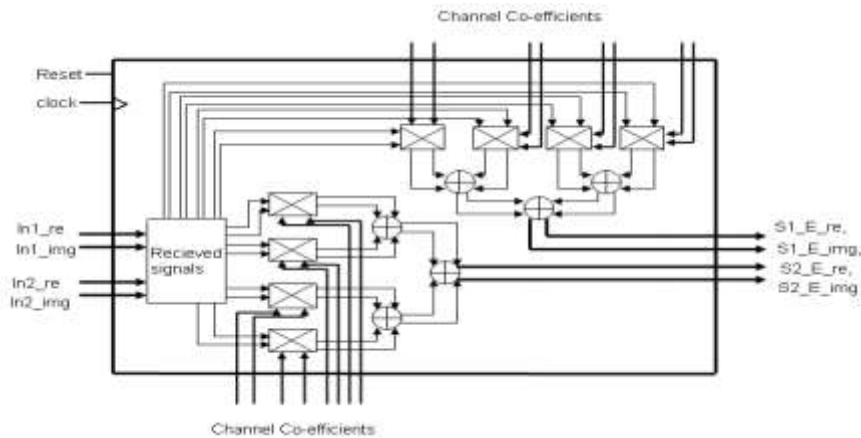
Figure 4.4: MIMO Decoder Module

The output of the wireless channel is fed to the MIMO Decoder, symbols transmitted from 2 antennas get added up at the receiver where in the decoder has to separate the symbols, Once the received signals are received after 2 time instances the decoder applies the following combiner equations.

$$s_1\_est = \quad \times \quad + \quad \times \quad + \quad \times \quad + \quad \times \quad \quad \ldots \quad (4.1)$$

$$s_2\_est = \quad \times \quad - \quad \times \quad + \quad \times \quad - \quad \times \quad \quad .. \quad (4.2)$$

The MIMO decoder gives out the S1 estimate and S2 estimate. The simulation results have been discussed in next section. The detailed schematic of the MIMO Decoder Module is shown in figure 4.4

The MIMO Decoder Module uses following resources

➢ 8 floating point complex multipliers
➢ floating point complex adders

The Design of QAM De-Modulator is not as simple as designing QAM Modulator. The output symbols coming from the MIMO decoder would have undergone Wireless Channel and the symbols are corrupted; the task of demodulator is to make a decision based on the minimum Euclidian distance. Verilog code is developed for the module

The wireless Channel is been modeled on hardware, the output's coming from MIMO encoder acts as input to Channel and the output of the channel acts as input to the MIMO decoder. Where it gets multiplied by the channel coefficients, and then gets added up before reaching the Receive Antennas
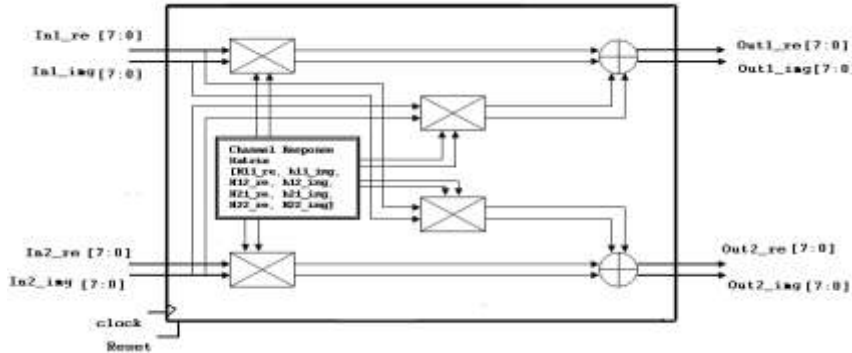

Figure 4.5: Wireless channel model

Symbols S1 and S2 get multiplied by channel coefficients and add up at the receiver refer figure 4.6. When two signals from two antennas are passed into the channel model it will replicate an actual wireless channel and give out added output, which acts as an input to MIMO decoder. It uses 4 complex multipliers and 2 complex adders, and the channel coefficients are stored in a memory, the values of channel co efficient come from channel estimator, when we are estimating the channel. The output of MIMO encoder passes through the wireless channel model and its output acts as input to MIMO decoder
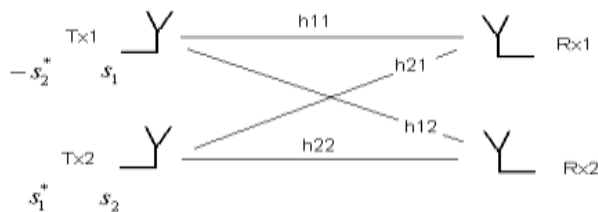

Figure 4.6: Wireless channel paths between antennas

5. Results

The coding for the entire MIMO System is done using Verilog HDL. In the following section simulation results and the synthesis results will be discussed.

The Number Format which is being used is floating point

Format, so it's very time consuming and hard to analyze the results, hence there was a need to develop a function which shows the equivalent representation of the floating point number, as shown in the f below.
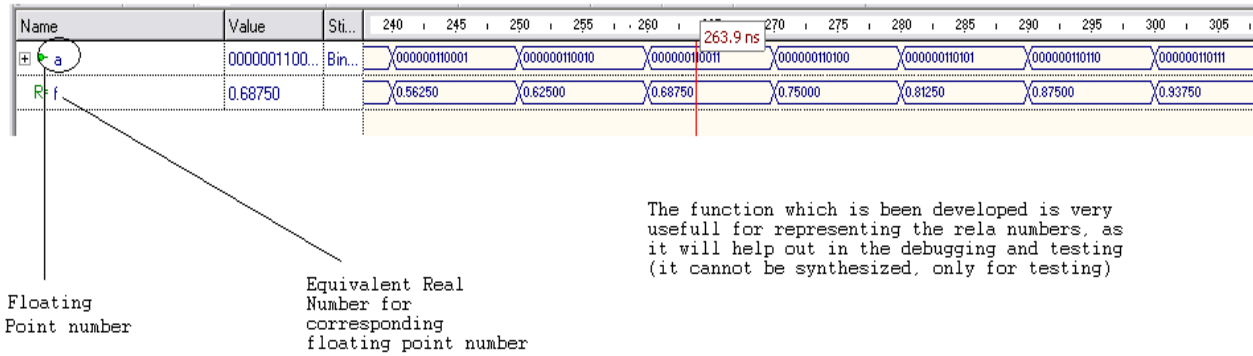

Figure 5.1:Float to real function simulation

For example

0000000110001 = 0.56250 as shown in simulation in figure 5.1

This makes the task easier for verification

➢ This is a function written in verilog
➢ This function is only used for verification of results and cannot be synthesized.
➢ We can plug in this function anywhere in the system and check the equivalent real values.
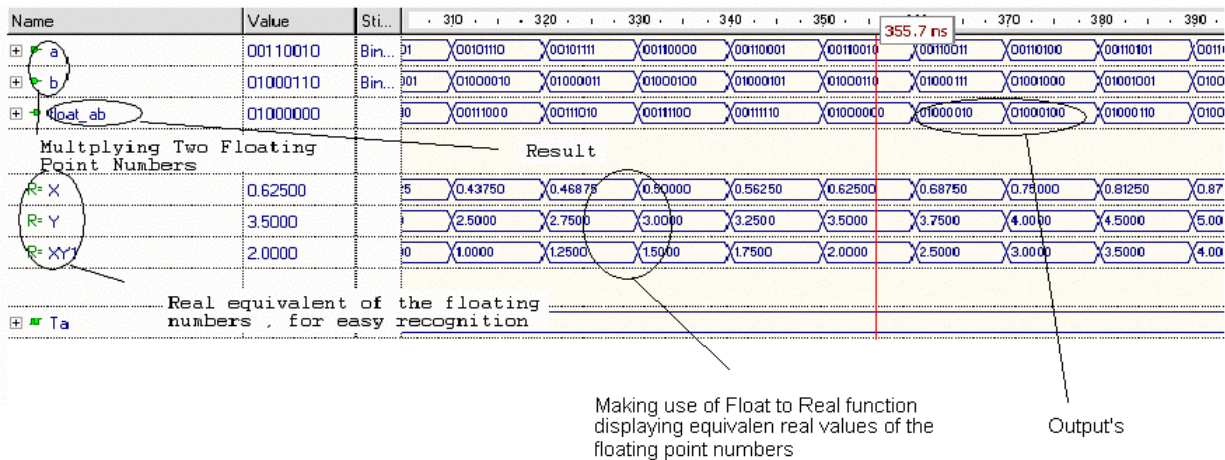
Below are the snapshots of simulation results

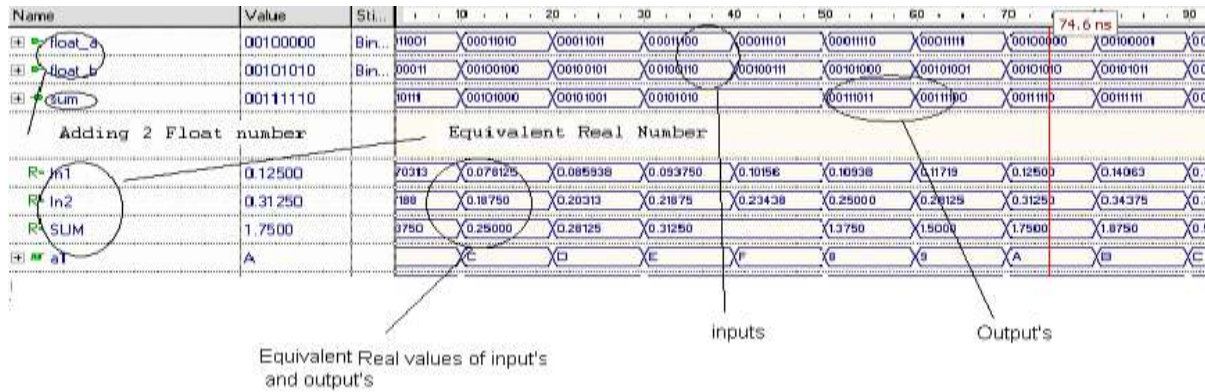Figure 5.2 Floating point Multiplier Simulation
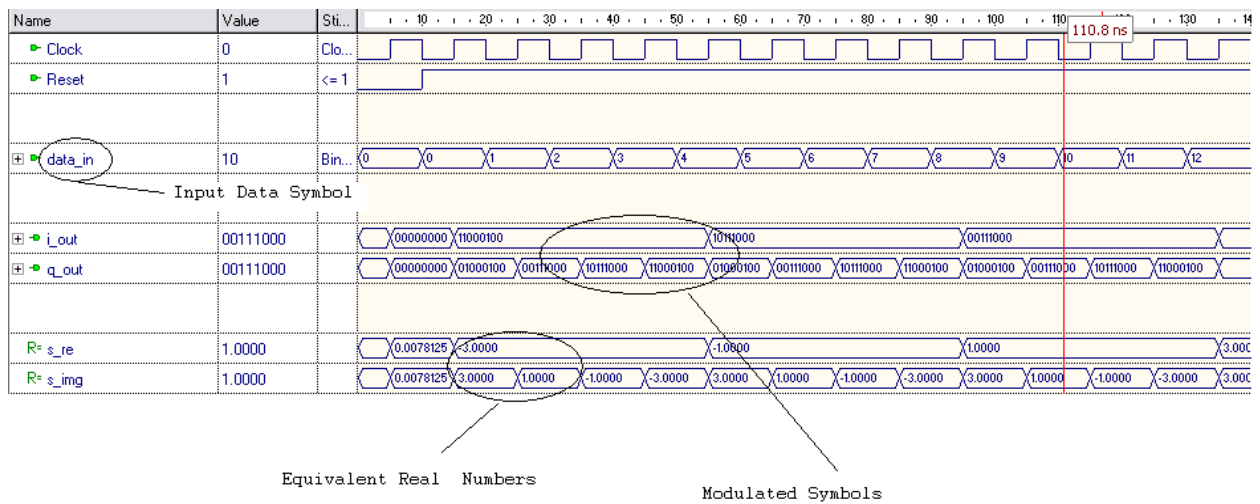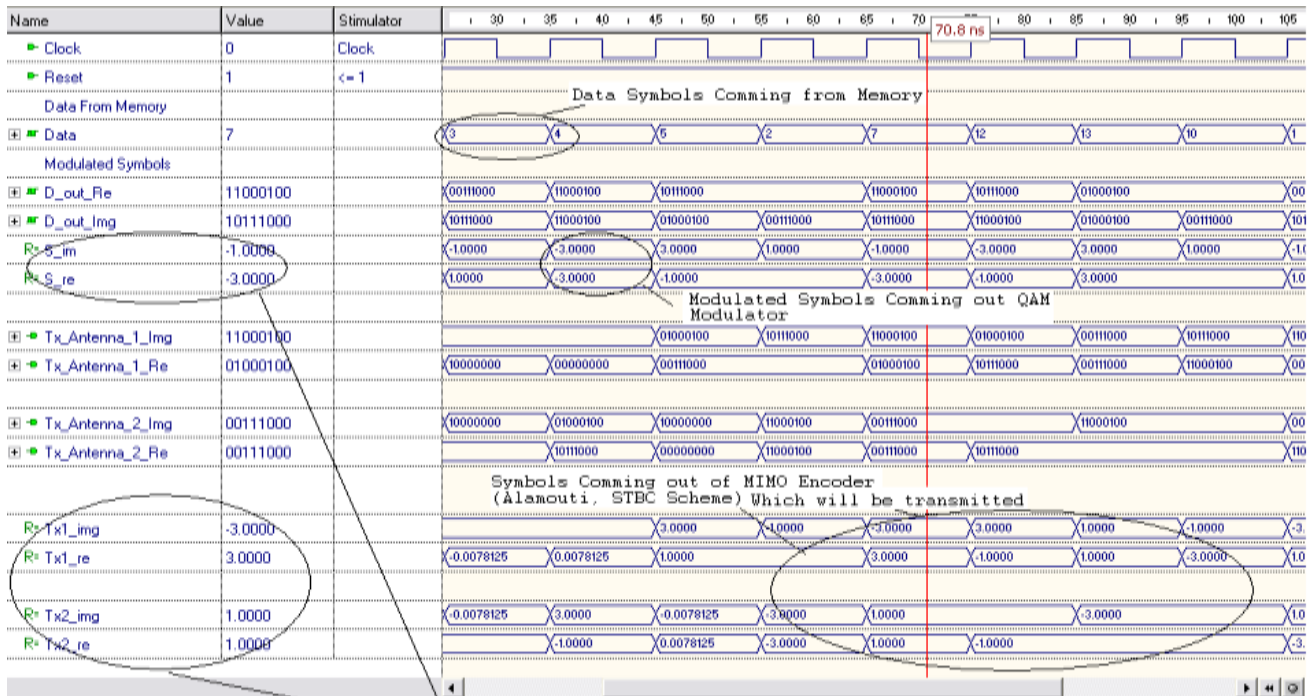
Figure 5.3 Floating point Adder Simulation

Figure 5.4: QAM Modulator Simulation
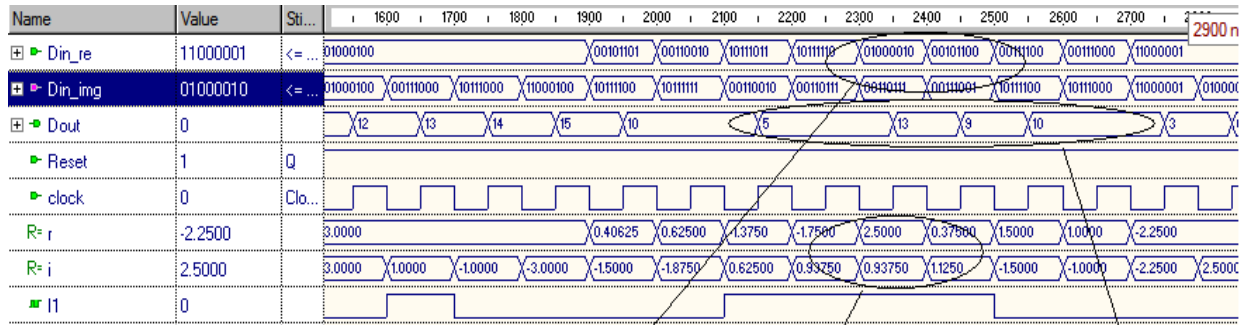
Figure 5.5: QAM Demodulator Simulation

Figure 5.6 MIMO Transmission simulations
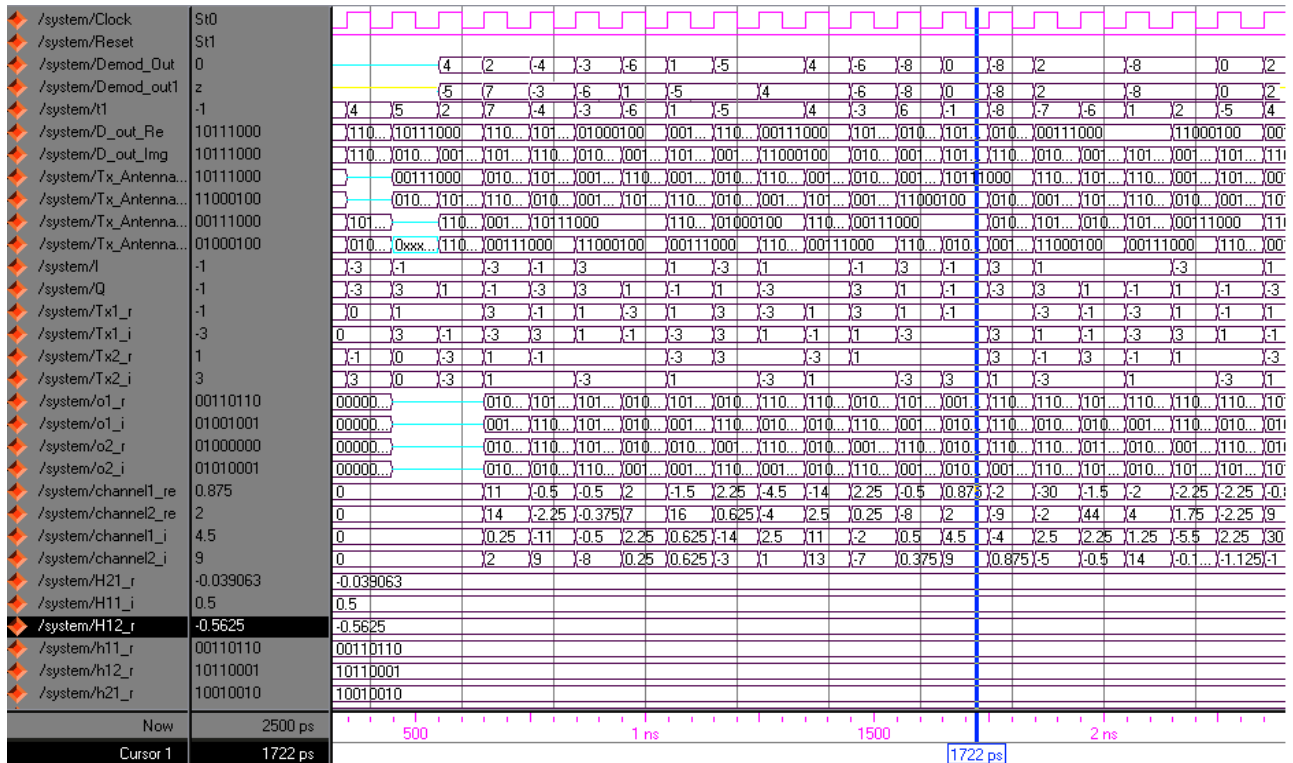
Figure 5.7: Top Level Simulation

Device Spartan 3 FPGA						
	Slices	Flip-Flops	4 input LUT's	IOB's	Block Rams	GClk's
Available Resources	1920	3840	3840	173	12	8
Resources Utilized by Each Module						
Input Memory	38 (1%)	32 (0%)	73 (1%)	6 (3%)	1 (8%)	1 (12%)
16 QAM Modulator	3 (0%)	12 (0%)	6 (0%)	22 (12%)	-	1 (12%)
MIMO STBC Encoder	111 (5%)	104 (2%)	203 (5%)	50 (28%)	1 (8%)	2 (25%)
MIMO STBC Decoder	1418 (73%)	96 (2%)	2532 (65%)	130 (75%)	-	3 (37%)
16 QAM Demodulator	15 (0%)	-	27 (0%)	22 (12%)	-	1 (12%)
Channel Model	1060 (55%)	-	1888 (49%)	65 (37%)	-	1 (12%)
Floating point Complex Multiplier	274 (14%)	-	490 (12%)	48 (27%)	-	1 (12%)
Floating Point Adder	71 (3%)	-	129 (3%)	24 (13%)	-	1 (12%)
Floating Point Multiplier	33 (1%)	-	59 (1%)	24 (1%)	-	1 (12%)

Table 1.Device utilization summary

6. CONCLUSIONS

The MIMO system design was discussed in detail, including all its modules. Verilog HDL code was written for all the modules within the system. Each individual module was tested for its correct functionality and then all the modules were integrated to form a one complete system.

An Optimized implementation of a MIMO system on an FPGA was done, the number representation used was IEEE floating point format unlike fixed point, which is most commonly used. Floating point and the results were discussed. Floating-point systems were developed to provide high resolution over a large dynamic range. Floating-point systems often can provide a solution when fixed-point systems, with their limited precision and dynamic range fail Floating-Point systems; however, bring a speed and complexity penalty. But we tried to reduce the complexity and increase the speed, by choosing a

custom floating point format. The results were discussed and the FPGA Resource utilization was discussed.

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